Active
- L1: (73) system-on-chip same core
- L2: (3) system-on-chip same core same (programmable adj5logic)
- L3: (70946) interfac$4 and (programmable adj5logic)
- L4: (38) l1 and l3
- L5: (10790) timing and constraint and array
- L6: (3) l4 and l5
- L7: (22) emulat$4 same core same (programmable adj5logic) same inte
- L8: (7) l7 and l5
- L9: (13) l7 and asic
- L10: (3) l8 and asic
- L11: (114304) application near9 circuit
- L16: (207) system-on-chip and core
- L17: (21) l3 and l5 and l16
- L18: (21839) interfac$4 same (programmable adj5logic)
- L19: (20) l17 and l18

Failed

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l17 and l18

🔘 BRS form 🔘 IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Title	Current OR	Curren
8	☑	☐	US 20010049757	20011206	Programmable task scheduler for use with multiport xDSL	710/33	
9	☑	☐	US 20010049756	20011206	Transport convergence sub-system with shared resources	710/33	
10	☑	☐	US 20010047465	20011129	Mixed hardware/software architecture and method for pro	712/43	
11	☑	☐	US 20010047434	20011129	xDSL communications systems using shared/multi-function	709/283	
12	☑	☐	US 20010037471	20011101	System and method for internal operation of multiple-po	713/600	
13	☑	☐	US 20010037443	20011101	Logical pipeline for data communications system	712/200	
14	☑	☐	US 6598128 B1	20030722	Microprocessor having improved memory management unit a	711/144	710/30
15	☑	☐	US 6591340 B2	20030708	Microprocessor having improved memory management unit a	711/118	711/14
16	☑	☐	US 6573905 B1	20030603	Video and graphics system with parallel processing of g	345/629	345/50
17	☑	☐	US 6553460 B1	20030422	Microprocessor having improved memory management unit a	711/125	711/20
18	☐	☐	US 6550042 B1	20030415	Hardware/software co-synthesis of heterogeneous low-pow	716/5	716/1;
19	☑	☐	US 6538656 B1	20030325	Video and graphics system with a data transport process	345/519	345/55
20	☑	☐	US 6412043 B1	20020625	Microprocessor having improved memory management unit a	711/118	711/14

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BRS: systems-on-chip
Pending
Active
L1: (148) core same (programmable adj3 logic) same interfac$3
L2: (4) 716/1-18.ccls. and l1 and asic
L3: (2797) timing near9 constraint
L4: (0) l2 and l3
L5: (24458) timing and constraint
L6: (2) l2 and l5
L7: (0) arithmetic and l6
L8: (0) alu and l6
L10: (2) array and l9
L11: (1) 6550042.pn.
L9: (2) calculat$4 and l6
L16: (5) systems-on
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array and l9

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Title	Current OR	Current
1	☐	☐	US 6550042 B1	20030415	Hardware/software co-synthesis of heterogeneous low-pow	716/5	716/1;
2	☐	☐	US 6377912 B1	20020423	Emulation system with time-multiplexed interconnect	703/28	716/1

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BRS: systems-on-chip
○ Pending
Active
L1: (148) core same (programmable adj3 logic) same interfac$3
L2: (4) 716/1-18.ccls. and l1 and asic
L3: (2797) timing near9 constraint
L4: (0) l2 and l3
L5: (24458) timing and constraint
L6: (2) l2 and l5
L7: (0) arithmetic and l6
L8: (0) alu and l6
L10: (2) array and l9
L11: (1) 6550042.pn.   ←
L9: (2) calculat$4 and l6
L16: (5) systems-on
Failed
Saved
Favorites
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Queue

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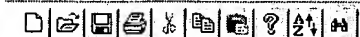Default operator: OR   ☑ Highlight all hit terms initially

systems-on

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	U	1	Document ID	Issue Date	Title	Current OR	Current
1	☐	☐	US 6457784 B1	20021001	Method and device for statically or dynamically determi	303/155	303/3
2	☑	☐	US 6175738 B1	20010116	Assigning channels of different capacities in a hybrid	455/451	370/468;
3	☑	☐	US 5910656 A	19990608	Adjustment of the sample support in time-of-flight mass	250/287	250/252.
4	☑	☐	US 5690869 A	19971125	Use of a polymer material on the basis of modified hydr	264/4.1	264/4.3;
5	☑	☐	US 5280557 A	19940118	Nonmaterial deflector-enhanced collector (NDC)	385/146	126/683;

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BRS: 17 same
- Pending
- Active
  - L5: (7677) programmable near9 interfac$4
  - L6: (10129) programmable same logic same implement$5
  - L7: (2368) timing near5 constraint
  - L8: (3045) merg$4 same design
  - L11: (117) programmable same logic same merg$5
  - L14: (24) 15 and 16 and 17
  - L15: (1) 15 and 16 and 17 and 18 *2001/0047509*
  - L17: (72) 17 same programmable
  - L20: (3) 114 and 117
- Failed
- Saved
- Favorites
- Tagged (0)
- UDC
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114 and 117

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	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☐	US 6467009 B1	20021015	64	Configurable processor system unit	710/305
2	☑	☐	US 6226757 B1	20010501	47	Apparatus and method for bus timing compensa	713/503
3	☐	☐	US 6226754 B1	20010501	48	Apparatus and method for device timing compe	713/400

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BRS: programmable same logic same merg$3
BRS: 17 same
BRS:
⊘ Pending
⊟ A Active
L3: (851) (programmable near9 logic) same (arithmet$4 or alu)
L4: (7688) programmable near9 interfac$4
L5: (118) programmable same logic same merg$5
L6: (1) 13 and 14 and 15
⊙ Failed
⊟ ⊚ Saved
(7677) programmable near9 interfac$4
(10129) programmable same logic same implement$5
(2368) timing near5 constraint
(3045) merg$4 same design
(117) programmable same logic same merg$5
(24) (programmable near9 interfac$4) and (programmable same l
(1) (programmable near9 interfac$4) and (programmable same lo

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13 and 14 and 15

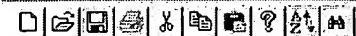BRS... IS&R... Im... Text HTML

U	1	Document ID	Issue Date	Pages	Title	Current OR
1		US 6052773 A	20000418	46	DPGA-coupled microprocessors	712/43

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